REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This Amendment is in response to the Office Action dated April 5, 2005. By the present amendment, the Specification and claims have been amended to respond to the 35 USC §112, second paragraph, rejection set forth on page 3 of the Office Action, as well as the objections to the Specification and claims set forth on page 2 and 3 of the Office Action. With regard to the amendment to claim 1, rejected under 35 USC §112, second paragraph, a correction has been made concerning the transistor type being referred to on lines 6 and 7. Therefore, it is respectfully requested that this clarification overcomes the 35 USC §112, second paragraph rejection, and removal of this rejection is respectfully requested. Similarly, removal of the objections to the Specification and claims set forth on pages 2 and 3 of the Office Action is also respectfully requested in light of the amendments made herein.

Briefly, the present invention is directed to an improved semiconductor device which includes both an NMOS and a PMOS field effect transistor. Referring to Fig. 4A-4E, an arrangement is shown in which a gate insulating film 5 is formed over the surface of a substrate having a p-type well area 3 and a n-type well area 4 in which the respective PMOS and NMOS transistors are to be formed (e.g., see page 9, lines 3 et seq.). A polycrystalline silicon region 6 (formed from an original amorphous silicon region, as described on page 12, line 9 et seq.) is formed over the gate insulator, with a layer of tungsten nitride (WNx) 9 and a layer of tungsten (W) 10 formed thereon.

Referring next to Fig. 1, an important feature of the invention is shown with regard to the segregation of the different type of dopants to different areas within the polycrystalline silicon film. In particular, as can be seen in Fig. 1, the n type impurity (e.g., phosphorus) used for doping the polycrystalline silicon for the NMOS transistor is segregated on the side of the interface between the polycrystalline silicon film and the gate insulator (that is, the gap area shown between the portion labeled POLY-Si and SiSUBSTRATE). On the other hand, the p-type impurity (e.g., boron) contained within the NMOS transistor is segregated to the side of the interface between the polycrystalline silicon film and the metallic nitride film (shown as WN in Fig. 1 towards the left-hand side of the figure). As explained on page 6, line 26 through page 7, line 6, this makes it possible to simplify the impurity doping process of the polycrystalline silicon film to realize a dual gate CMOS semiconductor device with reduced leakage of boron (or other p-type impurity) from the polycrystalline silicon film. In particular, as stated on page 7, lines 2-6:

> "That is, only one process for specifying a doping area makes it possible to form a dual gate and allow the boron in the polycrystalline silicon to be segregated on to the metallic nitride interface, thereby reducing the leakage."

Reconsideration and allowance of claims 1-10 over the prior art rejections based on Mogami (USP 5,656,519), Yang (USP 6,468,872) and Wristers (USP 5,674,788) is respectfully requested, whether these references are considered alone or in combination with one another. With regard to this, the Examiner apparently recognizes that neither Mogami, Yang nor Wristers teaches or suggests the claimed features set forth in the last paragraph of each of the independent claims 1 and 7. Taking claim 1 as an example, this last paragraph defines that the n-type impurity contained in the polycrystalline silicon film of the NMOS transistor is "segregated to a

side of an interface of the polycrystalline silicon film and said gate insulating film" while the P type impurity for the NMOS is "segregated to a side of an interface of said metallic nitride film and said polycrystalline silicon film." As discussed above, Fig. 1 clearly shows this segregation of the respective n-type impurity and p-type impurity on opposite sides of the polycrystalline silicon film. In other words, the n-type impurity is formed on one side of the polycrystalline silicon film adjacent to an interface of that polycrystalline silicon film with the gate insulating film while the p-type impurity for the NMOS transistor is segregated to the opposite side of the polycrystalline silicon film at the opposite interface of the polycrystalline silicon film with the metallic nitride film.

Notwithstanding the apparent recognition of this distinction over the cited prior art, page 5 of the Office Action states:

> "In regard to limitation concerning an n-type impurity segregated to a side of an interface of a polycrystalline silicon film and the gate insulating film, and a p-type impurity segregated to a side of an interface of a metallic nitride film and the polycrystalline silicon film, the semiconductor device structure as taught by Mogami and Yang is capable of having its impurities segregate to the interfaces claimed. The patentability of an apparatus is determined by its structure not how it functions."

Applicants respectfully submit that the claimed segregation of the respective impurities to different interfaces within the polycrystalline silicon film is clearly a structural difference, not a functional difference. This structural difference is clearly shown in Fig. 1 with the p-type impurity being formed on the left side of Fig. 1 (at the interface between the polycrystalline silicon layer and the metallic nitride layer WN) while the n-type impurity is segregated to the right side of the polycrystalline silicon film (at the interface with the gate insulator). There is nothing functional about this. It is, simply, a structural limitation regarding the impurity concentration of certain

impurities within the polycrystalline silicon film. Therefore, it is respectfully submitted that this reason for the rejection, based on the alleged function being claimed, is completely in error since the limitations in question in the last paragraph of each of claims 1 and 7 are structural, not functional.

In addition, it is respectfully submitted, that the semiconductor device structure as taught by Mogami and Yang "is capable of having its impurities segregate to the interface as claimed" goes completely against the specific requirements set forth in MPEP 2143.01 concerning "suggestion or motivation to modify the references." As set forth on page 131 in the May 2004 revision to MPEP 2143.01:

> "Fact that the claimed invention is within the capabilities of one or ordinary skill in the art is not sufficient by itself to establish *prima facie* obviousness."

Citing the case of Ex Parte Levengood, 28 USPQ 2d 1300 (Bd. Pat. App. & Inter. 1993), the MPEP states:

> "A statement that modifications of prior art to meet the claimed invention would have been "well within the ordinary skill of the art at the time the claimed invention was made" because the references relied upon teach that all aspects of the claimed invention are individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the references."

This falls within the general guidelines of MPEP 2143.01 which states, in the left hand column on page 130:

> "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art."

In the present instance, there is clearly no motivation within either Mogami or Yang (or in the secondary reference to Wrister for that matter) to provide the impurity segregation specifically required by each of the independent claims 1 and 7. As for

"knowledge generally available to one of ordinary skill in the art", MPEP 2144.03 clearly states:

> "While "official" notice may be relied on, these circumstances should be rare when an application is under final rejection or action under 37 CFR §1.113. Official notice unsupportive by documentary evidence should only be taken by the Examiner where the facts asserted to be well known, or to be common knowledge are capable of instant and unquestionable demonstration as being well known. "

As such, even if it were true that Mogami and Yang are "capable of having its impurities segregate to the interfaces claimed, " it is respectfully submitted that it certainly is not "capable of instant and unquestionable demonstration as being well known" as required by MPEP 2144.03. Thus, without specific motivation being provided documentary evidence, it is respectfully submitted that the position taken in the Office Action that it would be obvious to modify Mogami and Yang to meet the claimed limitations concerning the segregation of impurities is improper, and, accordingly, reconsideration and removal of the 35 USC §103 rejections based on these references and Wrister is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus,

LLP Deposit Account No. 01-2135 (Docket No. 500.38899VX4), and please credit any excess fees to such deposit account.

Respectfully submitted,
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